## REMARKS

The Office Action dated October 21, 2004, was carefully reviewed. The Examiner rejected claims 1-9 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,138,185 to Nelson et al. (hereinafter "Nelson") in view of U.S. Publication No. US2001/0025332 A1 to Wang et al. (hereinafter "Wang").

The Examiner asserted that Nelson discloses all of the limitations of claim 1 except synchronizing the serial I/O shifter using the clock signal. The Examiner asserted that Wang discloses the clock circuitry for a parallel channel that is shared by all of the data signals. The Examiner also asserted that the clock circuitry reduces the amount of power and physical space that is required to provide synchronized clocking. The Examiner asserted that it would have been obvious to combine Nelson with Wang to achieve the present invention.

The present invention requires a clock signal for clocking a transfer of *serial* data from the controller to the external device. The clock signal is for synchronizing the operation of the *serial* I/O shifter. The present invention teaches reconstructing serialized data for communication with a parallel device. Parallel reconstruction begins on the assertion of a latch signal to the external device. Thereafter, serial I/O data from the external device is clocked into the serial I/O shifter. Once all "n" bits of the serial I/O data stream have been clocked into the shifter, the shifter reconstructs the serial

data into parallel I/O signals. The parallel I/O signals are then output to the I/O crossover-switching network.

Wang does not teach or disclose a clock signal for synchronizing the transfer of serial data from the controller to the external device where the clock signal synchronizes the operation of the I/O shifter as taught by the present invention. The Wang reference teaches that the parallel channels transfer the communications in parallel with a clock signal and teaches away from serial clocking, see paragraph [0013]. In the Wang reference, see paragraph [0029], communication processing circuitry share clock information over parallel channels. A parallel channel transfers communications in multiple parallel bit streams. The parallel channel also transfers the clock signal that is parallel to the bit streams for the communications. The present invention teaches, and claims "serially transferring bits of the data stream from an I/O multiplexer to an external device at the rate of one bit per cycle of a clock signal."

If Wang were combined with the Nelson, it would not result in the Applicants' invention because Wang teaches away from serially transferring bits at the rate of one bit per cycle of a clock signal. Nelson teaches processing connection and clear requests concurrently to avoid blocking signals at busy ports. The clock signal is Nelson is used to encode requests and is not used to synchronize the I/O shifter as claimed in the present invention. Wang discloses a parallel communication circuit that synchronizes parallel channels. Because neither the Nelson reference nor the Wang reference teach

synchronization of the clock signal and the serial I/O shifter, the combination of Nelson and Wang would not result in a synchronous transfer of serial data and reconstruction of parallel I/O signals from an incoming serial data stream as taught by the Applicant of the present invention.

It is also respectfully asserted that one skilled in the art would not look to combine Nelson and Wang to accomplish the Applicants' invention as suggested by the Examiner. Wang teaches away from serial transfer and a clock signal for synchronizing serial transfer. One skilled in the art would not look to combine Wang, which is directed to parallel transfer and teaches away from serial transfer, to accomplish the invention as claimed by the applicant of the present invention which is to synchronize the transfer of serial data.

Regarding claim 5, and the claims that depend therefrom, the Examiner asserted that Nelson discloses serially transferring bits of the data stream from an I/O multiplexer to an external device at the rate of one bit per cycle of a clock signal at column 4, lines 45-61. It is respectfully asserted that Nelson does not teach or disclose transferring bits of the data stream at the rate of one bit per cycle of a clock signal and does not teach or disclose transferring bits of the data stream from an I/O multiplexer to an external device at the rate of one bit per cycle of a clock signal.

The Nelson reference discloses each PRC receives a serial bit stream on one of the connections lines within the request portion of the connection bus. When a request on a bus is detected by a particular PRC, the PRC decodes the request type and verifies the request's check bit. However, the clock signal in

Nelson does not synchronize the I/O shifters with an external device and does not teach a mandatory timing relationship between the connection and the response buses as taught by the Applicants of the present invention. In Nelson, the serial request and response buses operate independently in a non-blocking fashion to process connection and clear requests in parallel.

Further, at column 4, lines 5-17, Nelson emphasizes that each serial request bus and each serial reply bus are independent, requests and responses can be processed concurrently to reduce latency. Nelson defines "concurrently" as meaning "processed during a single clock cycle." The clock signal in Nelson is not used to serialize parallel data and does not serially transfer bits of the data stream to an external device at the rate of one bit per cycle as taught by the Applicants of the present invention.

It is respectfully requested the Examiner withdraw the rejection of claims 1-9 under 35 U.S.C. § 103. Should the Examiner have any questions or comments that may place the application in better condition for allowance, he is respectfully requested to call the undersigned attorney.

Respectfully submitted,

Angela M. Brunetti

Angela M. Brunetti
Reg. No. 41,647

Attorney for Applicant(s)

Date: November 29, 2004

Artz & Artz, P.C.
28333 Telegraph Road, Suite 250
Southfield, MI 48034
(248) 223-9500
(248) 223-9522 (fax)